

REMARKS

Claim 1 has been amended and claim 25 has been previously canceled. Claims 1 to 7, 13 to 16 and 23 remain active in this application, claims 8 to 12, 17 to 22 and 24 have been withdrawn and claim 25 has been canceled.

Claims 1 to 7, 13 to 16 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Boudreaux, Jr.(U.S. 6,668,060) in view of Anderson et al. (U.S. 6,728,37)). The rejection is respectfully traversed.

As stated at page 3, lines 12ff, one embodiment of the low power SLIC is implemented by having two current sources in parallel (one high efficiency, the other high fidelity) as illustrated by Figure 10. The DC current source has high efficiency and a high impedance in the voice band, while the AC current source synthesizes a 600 Ohm (typical) termination and does the high fidelity speech transmit and receiving (hybrid) functions. The DC current source then is optimized for efficiency while the AC current source is optimized for fidelity (voice band performance). As stated at page 11, line 4ff, the DC current source has high efficiency of from 85% to 90%. No such concepts are taught or even remotely suggested by Boudreaux, Jr, Anderson et al. or any proper combination of these references. This concept is embodied in claim 1. The Office action fails to show where either reference or any proper combination thereof shows the combination of a DC current source in parallel with an AC current source, let alone the other features of these sources as claimed.

Claims 2 to 7 depend from claim 1 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 1.

Claim 2 further limits claim 1 by requiring that the DC current source comprise a switched-mode current boost converter. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 1 are to be found.

Claim 3 further limits claim 2 by requiring that the switched-mode current boost converter comprise a first semiconductor switch and a second semiconductor switch, the first and second semiconductor switches configured such that when the first semiconductor switch is open, the second semiconductor switch is closed to implement a first state, and such that when the first semiconductor switch is closed, the second semiconductor switch is open to implement a second state. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 2 are to be found.

Claim 4 further limits claim 3 by requiring that the switched-mode current boost converter further comprise a capacitor configured to be charged by a current source when the first and second semiconductor switches are in the first state, and further configured to be discharging when the first and second semiconductor switches are in the second state. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 3 are to be found.

Claim 5 further limits claim 4 by requiring that the switched-mode current boost converter further comprise a series inductor at its output, operational to achieve the high impedance in a subscriber line voice band, and having an inductance sufficient to limit converter output current ripple to less than about one percent. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 4 are to be found.

Claim 6 further limits claim 5 by requiring that the first semiconductor switch comprise a CMOS transistor that is operational in response to a dynamically time varied input signal to cause the switched-mode current boost converter to switch between its first and second states to maintain a constant output current. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 5 are to be found.

Claim 7 further limits claim 6 by requiring that the second semiconductor switch comprise a fast response diode that is operational to switch alternately and in complimentary fashion with the CMOS transistor in response to the dynamically time varied input signal. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 6 are to be found.

Claim 13 requires, among other features, a switched-mode current boost converter configured to provide a constant DC current feed to a subscriber line. No such

combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim are to be found.

Claim 13 further requires a first switch and a second switch, the first and second switches responsive to a dynamically time varied input signal to switch alternately and in complementary fashion to implement a first state and a second state such that the at least one capacitor is charged by a current source while in the first state and discharging via the at least one output series inductor in the second state to generate the constant DC current feed. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim are to be found.

Claims 14 to 16 depend from claim 13 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 13.

In addition, claim 14 further limits claim 13 by requiring an AC current source configured to synthesize a subscriber line termination impedance and to implement subscriber line high fidelity speech transmit and receiving functions. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 13 are to be found.

Claim 15 further limits claim 13 by requiring that the first switch comprise a CMOS transistor in response to the dynamically time varied input signal to cause the switched-mode current boost converter to switch between its first and second states to maintain a constant DC output current. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 13 are to be found.

Claim 16 further limits claim 15 by requiring that the second switch comprise a fast response diode to switch alternately and in complimentary fashion with the CMOS transistor in response to the dynamically time varied input signal. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim or the combination with claim 13 are to be found.

Claim 17 further limits claim 13 by requiring that the dynamically time varied input signal be generated via a pulse width modulated controller. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references since there is no showing how the combination is to be found in the cited references.

Claim 23 requires, among other features, a method of generating a subscriber line constant DC current feed. No such combination is taught or suggested by Boudreaux, Jr., Anderson et al. or any proper combination of these references

Claim 23 further requires, among other features, the steps of charging the capacitor via a current source for a first time period in response to a dynamically time

variable input signal and discharging the capacitor via the series output inductor for a second time period in response to the dynamically time variable input signal such that there is substantially no change of energy in the inductor and the capacitor to generate a constant DC output current to the subscriber line, the DC output current having a magnitude greater than the source current operative to charge the capacitor. Nowhere in the Office action is there any attempt to show where in the cited art the features of this claim are to be found.

With reference to the allegation that the arguments fail to comply with 37 C.F.R. 1.111(b), this allegation is very strongly traversed. The response could not be more specific. The response refers specifically to features in the claims which are stated not to be shown in the prior art and these arguments have not only not been refuted, but have been ignored.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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